
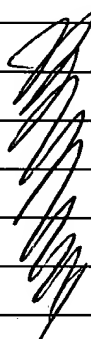


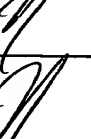


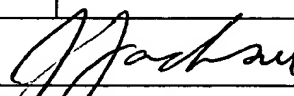


Form PTO-1449 (REV. 8-83)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 036654 D		APPLICATION NO. Rule 1.53(b) Continuation of U.S. Patent Application No. 09/373,982  <div style="font-size: 1.5em; font-weight: bold;">885027</div>	
INFORMATION DISCLOSURE STATEMENT  (Use several sheets if necessary)				APPLICANT Mitsutoshi MIYASAKA		FILING DATE June 21, 2001	
				GROUP			

11033 U.S. PTO  
09/885027  
86/21/01

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
		5,192,717	03-93	KAWAKAMI		
		5,289,030	02-94	YAMAZAKI		
		5,372,958	12-94	MIYASAKA		
		5,482,749	01-96	TELFORD		
		5,488,000	01-96	ZHANG		
		5,624,873	04-97	FONASH		
		5,648,276	07-97	HARA		
FOREIGN PATENT DOCUMENTS						
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
		JP-A-6-132306	05-94	JAPAN		
		JP-A-58-164267	09-83	JAPAN		
		JP-A-5-55582	03-93	JAPAN		
		JP-A-4-245482	09-92	JAPAN		
		JP-A-59-204275	11-84	JAPAN		
		JP-A-4-7843	01-92	JAPAN		
		JP-A-6-97079	04-94	JAPAN		
		JP-A-63-115328	05-88	JAPAN		
		JP-A-2-137797	05-90	JAPAN		
		JP-A-6-232059	08-94	JAPAN		
		JP-A-6-16-3401	08-94	JAPAN		
		JP-A-6-275524	09-94	JAPAN		
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)						
		Ohshima, H., et al. "Full-Color LCDs with Completely Integrated Drivers Utilizing Low-Temperature Poly-Si TFTs", <u>SID 93 DIGEST</u> 1993, PP. 387-390.				
		S. Wolf, et al., "Silicon Processing for the VLSI Era Vol 1, Lattice Press, 1986 (month not available)"				
EXAMINER 				DATE CONSIDERED <div style="font-size: 1.5em; font-weight: bold;">8/02</div>		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						

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				FILING DATE June 21, 2001		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	
		4,297,392	10-81	HIGASHI et al.			
		5,313,075	05-94	ZHANG et al.			
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	
		EO 0 254 589 A2	07-87	EUROPEAN PATENT OFFICE			
		EP 0 552 375 A1	07-92	EUROPEAN PATENT OFFICE			
		EP 0 526 779 A1	07-92	EUROPEAN PATENT OFFICE			
		EP 0 562 623 A2	03-93	EUROPEAN PATENT OFFICE			
		EP 0 592 227 A2	10-93	EUROPEAN PATENT OFFICE			
		EP 0 598 394 A2	11-93	EUROPEAN PATENT OFFICE			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
		Masatada Horiuchi et al, "One-Decade Reduction of PN-Junction Leakage Current Using Poly-SI Interlayered SOI Structures" Proceedings of the International Electron Devices Meeting, Wash, DC 12/5-8/1993.					
		5 December 1993, Institute of Electrical and Electronics Engineers, pgs. 847-850, XP000481744					
		Masumo K et al., "Low-Temperature Preparation of Poly-SI TFT by AR Laser Annealing at High Scanning Speed"					
		Electronics & Communications in Japan, Part II - Electronics, vol. 76, no. 9, 1 Sept. 1993, pgs. 112-116, XP000447931.					
		Yeckel, A. et al, "The Origin of Nonuniform Growth of LPCVD films from silane gas Mixtures" Journal of the					
		Electrochemical Society, July 1989, vol. 136, no. 7, ISSN 0013-4651.					
		Mitsutoshi Miyasaka et al, "Transistor and Physical Properties of Polycrystalline Silicon Films Prepared by Infralow-					
		Pressure Chemical Vapor Deposition", Journal of Applied Physics, vol. 74, no. 4, 15 Aug. 1993, pgs 2870-2885.					
		Patent Abstracts of Japan, vol. 018, no. 573 (E-1624), 2 Nov. 1994 & JP 06 216004 A (NEC Corp), 5 Aug. 1994					
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					<b>8/02</b>		
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U.S. PATENT DOCUMENTS						
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
		5,583,369	12-96	YAMAZAKI et al.		
		5,114,770	05-92	ECHIZEN et al.		
		4,812,328	03-89	SAITOH et al.		

FOREIGN PATENT DOCUMENTS						
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		

EXAMINER  	DATE CONSIDERED  <b>8/02</b>
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